

## **AMENDMENTS TO THE CLAIMS**

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Original) A non-volatile memory cell comprising:  
  
a device isolation layer disposed in a substrate to define an active region;  
  
a floating gate disposed over the active region and comprised of a plurality of first conductive patterns and a plurality of second conductive patterns which are alternately stacked; and  
  
a first insulation layer interposed between the floating gate and the active region, wherein one of the first and second conductive patterns protrudes to form concave and convex shaped sidewalls of the floating gate.
2. (Original) The non-volatile memory cell of claim 1, wherein one of the first and second conductive patterns is formed of doped polysilicon layers and the other of the first and second conductive patterns is formed of doped silicon germanium layers.
3. (Original) The nonvolatile memory cell of claim 2, wherein the doped polysilicon layers protrude to form convex portions of the sidewalls of the floating gate and the doped silicon germanium layers forms concave portion of the sidewalls of the floating gate.
4. (Original) The non-volatile memory cell of claim 1, further comprising:  
  
a control gate electrode disposed over the floating gate and crossing over the active region; and  
  
a gate interlayer dielectric pattern disposed between the control gate electrode and the floating gate,

wherein the gate interlayer dielectric pattern and the control gate electrode are disposed over a top surface and the concave and convex sidewalls of the floating gate.

5. (Original) The non-volatile memory cell of claim 4, further comprising impurity diffusion layers formed in the active region at sides of the control gate electrode.

6. (Original) The non-volatile memory cell of claim 4, further comprising:  
a selection gate pattern crossing over the active region at one side of the control gate electrode;

a floating impurity diffusion layer disposed in the active region between the selection gate pattern and the control gate electrode; and

an impurity diffusion layer respectively formed in the active region that is beside the selection gate pattern and opposite to one side of the floating impurity diffusion layer, and in the active region that is beside the floating gate and opposite another side of the floating impurity diffusion layer,

wherein a portion of the floating impurity diffusion layer overlaps a portion of the floating gate.

7. (Original) The non-volatile memory cell of claim 6, further comprising:  
a tunnel window region including a predetermined bottom region of the floating gate and the active region thereunder; and

a second insulation layer disposed between the floating gate and the active region in the tunnel window region,

wherein the tunnel window region is disposed in the overlapping region of the floating gate and the floating impurity diffusion layer, and the second insulation layer is thinner than the first insulation layer.

8. (Original) The non-volatile memory cell of claim 6, wherein the selection gate pattern comprises a first selection gate electrode, a selection gate dielectric pattern and a second selection gate electrode,

wherein the first selection gate electrode is formed of the same material layer as the floating gate, the selection gate dielectric pattern is formed of the same material layer as the gate interlayer dielectric pattern, and the second selection gate electrode is formed of the same material layer as the control gate electrode.

9-19. (Canceled)

20. (Currently Amended) A non-volatile memory cell comprising:

a substrate;

an active region formed in the substrate; and

a floating gate having sidewalls formed over the active region, the sidewalls having protruding portions, wherein the floating gate comprises a plurality of first conductive patterns and a plurality of second conductive patterns.

21. (Canceled)

22. (Currently Amended) The non-volatile memory of claim ~~21~~ 20, wherein one of the plurality of first conductive patterns and the plurality of second conductive patterns forms the protruding portions of the sidewalls of the floating gate.

23. (Original) The non-volatile memory of claim 20, wherein one of the plurality of first conductive patterns and the plurality of second conductive patterns is formed of doped polysilicon layers and the other of the plurality of first conductive patterns and the plurality of second conductive patterns is formed of doped silicon germanium layers.

24. (Original) The non-volatile memory of claim 23, wherein the doped polysilicon layers form the protruding portions of the sidewalls.

25-28. (Canceled)